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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,682	06/09/2000	Sheila M. Rader	CS-10246	3605

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Motorola inc
Personal Communications Sector
Intellectual Property Department (MCS)
600 North US Highway 45 AN475
Libertyville, IL 60048

EXAMINER
THAI, XUAN MARIAN

ART UNIT	PAPER NUMBER
2181	8

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/591,682	RADER ET AL.	
	Examiner	Art Unit	
	XUAN M. THAI	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *17-28 and 35-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4 &7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This is in response to an election of claims in a Restriction Requirement filed on April 14, 2003. Applicants elected claims 1-16 and 29-34 to be prosecuted in the present application. Claims 17-28 and 35-37 are withdrawn from further consideration as being directed to non-elected inventions.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Heath et al. (USPN 4,901,234; hereinafter Heath).

As per claim 1, Heath discloses the claimed invention including a data transfer system comprising: a plurality of peripheral interfaces [inherently taught in Heath in that Heath discloses a plurality of peripheral devices e.g. optical disk 21, floppy disks 22 and 23, comm. Devices 18 and 19; fig. 1]; a first memory [main memory 15 or aux. Memory 17]; and a programmable direct memory access module [DMA controller 12] coupling the first memory [15 or aux. Memory 17] to each of the plurality of peripheral interfaces [coupling the plurality of peripheral devices through bus 25], wherein the programmable direct memory access module configures

selectively programmable direct memory access channels between the first memory [15 or aux. Memory 17] and respective ones of the plurality of peripheral interfaces [e.g. see fig. 1; see also Abstract; col. 3, lines 17-60];

As per claim 2, further comprising a first processor [processor 10] coupled to the programmable direct memory access module [dma controller 12] and associated with the first memory [15 or 17; see fig. 1];

As per claim 3, further comprising a second memory [e.g. 15 or memory 17] coupled to the programmable direct memory access module [dma controller 12], wherein the PDMA module configures the selectively dma channels between the second memory and the respective ones of the plurality of peripheral interfaces [see col. 3, lines 17-60];

As per claim 4, further comprising a second processor [e.g. math co-processor 14] coupled to the PDMA module [dma controller 12] and associated with the second memory [e.g. memory 15 or 17; see fig. 1];

As per claim 5, further selectively programmable dma data channels are configured between the first memory and the second memory is disclosed in Heath in that Heath states that the aux. Memory 17 is granted dma access channel by the dma controller to perform DMA access [col. 3, lines 17-60];

As per claim 6, wherein the dma module [dma controller 12] includes a programmable processor [processor 10];

As per claim 7, wherein the PDMA module further includes a dma controller 12 coupled to the programmable processor 10, wherein the processor 10 configures the selectively

programmable dma channels between the first memory [15 or 17] and the peripheral interfaces [e.g. optical disk 21, floppy disks 22 and 23, comm. Devices 18 and 19] via a dedicated dma data transfer channel of the dma controller [see col. 3, lines 17-60; see also col. 5, lines 50 et seq. bridging col. 6, lines 1-27];

As per claim 8, the dma module further comprises a scheduler [arbiter] for prioritizing data transfers over the respective ones of the selectively programmable data channels [see col. 6, lines 11-20];

As per claim 9, Heath discloses the claimed invention including a direct memory access system comprising: a dma controller [12] establishing dma data channel and including a first interface [e.g. interface for memory 17 or 15] for coupling to a memory [see fig. 1]; a second interface [e.g. dma slave 24; see col. 3, lines 26-32]; and a processor [10] coupled to the dma controller 12 and coupled to the second interface [e.g. 25] wherein the processor configures dma data channel to transfer data between a programmable selectable respective one or more of the plurality of nodes and the memory [17 or 15; see col. 3, lines 17-60 and col. 5, lines 50 et seq. bridging col. 6, lines 1-27];

As per claim 10, wherein the plurality of nodes are one of the plurality of peripheral interfaces and a memory interface [see fig. 1];

As per claim 11, further comprises a scheduler [arbiter] for prioritizing data transfer via the dma channel according to predetermined priorities [see col. 6, lines 11-20];

As per claim 12, Heath discloses the method for performing dma, the method comprising: receiving a request for dma transfers [see col. 3, lines 44-45]; configuring code to establish a dma data channel between a node and a dma interface [see col. 4, lines 7-20; col. 6, lines 2-20];

transferring data between the node and the dma interface along the direct memory access data channel [col. 6, lines 2-20];

As per claim 13, wherein the receiving step comprises receiving a timed request for a dma transfer [see col. 4, lines 34, 59-60];

As per claim 14, further comprising: prioritizing data [e.g. see col. 4, lines 5-20].

4. Claims 29-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Garde et al. (USPN 5,634,076; hereinafter Garde).

As per claim 29, Garde discloses a processor communication system comprising: a host processor dma interface [e.g. DSP or core processor or I/O processor]; one or more peripheral ports [abstract, lines 19-21]; a data bus [e.g. 162]; and a programmable controller [100] comprising a plurality of registers [e.g. FIFO buffers or registers 124] in communication with said data bus for maintaining data communication, with the controller being operable for storing and retrieving data from the plurality of registers to establish multiple data transfers between said host processor interface and one or more peripheral ports [fig. 2, see col. 5, lines 42-53];

As per claim 30, Garde discloses a second processor [e.g. I/O processor or DSP] interface, wherein the programmable controller [dma controller 100] is operable for establishing multiple data transfers between the host and the second interfaces and one or more peripheral ports [see col. 5, lines 22-65; col. 12, lines 32 et seq. bridging col. 13, lines 1-40];

As per claim 31, Garde discloses wherein the programmable processor prioritizes the multiple data transfers by storing and retrieving data from a plurality of registers [FIFO buffers; e.g. col. 11, lines 50-65; col. 13, lines 20-23; col. 14, lines 20-40];

As per claim 32, Garde discloses wherein a second processor interface comprising a DSP dma interface [dma controller 100];

As per claim 33, wherein the programmable controller is operable for establishing multiple virtual dma channels [col. 13, lines 1-25];

As per claim 34, comprising embedded dma memory for use with host processor [e.g. internal memory 16; col. 15, lines 44-46];

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heath et al. (USPN 4,901,234; hereinafter Heath) in view of Kamiya (USPN 5,809,335).

As per claims 15 and 16, Heath discloses the claimed invention except for being silent on the method of interrupting and resuming the transferring of data in the event a higher priority dma data transfer is required. Kamiya discloses that it is known at the time the invention was made to provide a capability in dma data transfer to interrupt and resume the transfer of data through a channels such that the lower priority data transfer is interrupted so the higher priority data transfer can take place [see abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the capabilities for interrupting and resuming the lower priority dma data transfer as taught by Kamiya in the Heath system in that Kamiya states that by providing the apparatus with capability of carrying out interruption and resumption of DMA block transfer, important data that have urgent need can be efficiently transfer in an efficient and prompt manner [see col. 1, lines 5-12, and 44-48].

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached form PTO-892.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Flexible Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

XUAN M. THAI
Primary Examiner
Art Unit 2181

XMT
May 19, 2003